REMARKS

We acknowledge the Examiner's indication that claims 2, 5, 7, 9, 12, 14 and 16 would be allowable if amended to be in independent form and to include all of the limitations recited in any base and intervening claims. We submit however that we are entitled to greater protection than that offered by these claims. We have also amended independent claim 1 to provide proper antecedent basis to the phrase "control voltage."

Prior Art Rejections

Independent Claims 1 and 8

The Examiner rejected independent claims 1 and 8 as being anticipated by Ho (U.S. Patent 5,363,419). Claims 6 and 13 were rejected as being unpatentable over Ho.

We submit that Ho does not disclose "a second loop generating the control voltage at a constant value and supplying the voltage controlled oscillator with the constant control voltage until the difference between the frequency of the first reference signal and the frequency of the clock signal converges to within a predetermined range," as recited in independent claims 1 and 8. Rather, Ho discloses a dual phase-locked-loop having a digital control circuit 2 which disables the contribution of current I_A from an analogue circuit 1 when the digital circuit senses that the VCO frequency is out of range. Specifically, when the VCO frequency is out of range, the digital control circuit 2 activates LOCK and LOCKN signals to provide a voltage VD to FETs 34, 37 so that $I_A = 0$. But, Ho says nothing about the voltage supplied to VCO 4 being a constant voltage until the difference between the frequency of a first reference signal and the frequency of a clock signal converges to within a predetermined range in a first loop.

The Examiner also rejected dependent claims 3-4, 6, 10-11, and 13 as unpatentable over Ho. Because claims 3-4 and 6 depend from independent claim 1 and claims 10-11 and 13 depend from independent claim 8, we submit that these claims are patentable for at least the same reasons that claims 1 and 8 are patentable.

Independent Claim 15

The Examiner rejected independent claim 15 as being anticipated by Ho. Dependent claim 17 was also rejected as being unpatentable over Ho.

We submit that Ho does not disclose a method for controlling a voltage controlled oscillator of a PLL circuit, the method comprising controlling the phase of the clock signal including generating the control voltage at a constant value and supplying the voltage controlled oscillator with the constant control voltage until the difference between the frequency of the first signal and the frequency of the clock signal converges to within a predetermined range, as recited in independent claim 15. As discussed above, Ho says nothing about the voltage supplied to VCO 4 being a constant voltage until the difference between the frequency of a first reference signal and the frequency of a clock signal converges to within a predetermined range in a first loop.

Because claim 17 depends from independent claim 15, we submit that it is patentable for at least the same reason that claim 15 is patentable.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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